United States Patent Office

3,404,295

Patented Oct. 1, 1968

3,404,295

HIGH FREQUENCY AND VOLTAGE TRANSISTOR WITH ADDED REGION FOR PUNCH-THROUGH PROTECTION

Raymond M. Warner, Jr., Scottsdale, Ariz., assignor to Motorola, Inc., Franklin Park, Ill., a corporation of Illinois

Filed Nov. 30, 1964, Ser. No. 414,525
15 Claims. (Cl. 307—302)

ABSTRACT OF THE DISCLOSURE

A semiconductor structure having a pair of rectifying junctions respectively separating regions of opposite conductivity type materials, with one junction being of greater extent than the other. A lock region having a conductivity type of the intermediate region is embedded in the region adjacent the longer junction and extends in spaced parallel relationship to that junction for limiting the penetration of any depletion layer toward said second junction thereby preventing voltage punch-through of the intermediate region. The lock region extends only partially across the semiconductor structure.

This invention relates generally to transistors, and more particularly to a transistor which provides improved high power, high frequency operation.

High power transistors which have been provided in the past have not been suitable for high frequency operation. Further, such high power transistors have not had constant gain over a large voltage range, and have provided low gain at low voltages and higher gain at higher voltages. This is because in order to withstand high voltages, it is necessary that the base region of the transistor be relatively thick. However, when high voltage is applied to the collector region of the transistor, the collector depletion layer extends into the base region to effectively reduce the base thickness. When the operating voltage is increased so that the collector depletion layer reaches the emitter electrode, objectionable punch-through takes place. Because of the requirement of a relatively thick base region to prevent punch-through at high voltage operation, the carriers therein have a longer distance to travel and at low voltage a large number of the carriers are dissipated to reduce the gain. When higher voltage is applied, the collector depletion area extends into the base region so that the distance of carrier travel is shorter and fewer carriers are lost, so that the gain increases.

Another problem with high power transistors is that known structures are not suitable for high frequency operation. This is because the collector-base capacitance is relatively high. Also, the thick base requires long transit time for the carriers, which limits the high frequency response.

It is therefore an object of the present invention to provide an improved high power, high frequency transistor.

Another object of the invention is to provide a high voltage, high gain transistor, wherein the gain remains substantially constant over a wide range of operating voltages.

A further object is to provide a transistor which can be operated over a wide range of voltages without causing punch-through between the collector depletion layer and the emitter region.

A still further object of this invention is to provide a transistor which operates in a manner analogous to the operation of a vacuum tube.

A more specific object of the invention is to provide a transistor in which the extent of the collector depletion layer into the base region is controlled.

A feature of the invention is the provision of a transistor having emitter and collector regions separated by a base region, wherein the collector region includes a lock layer for controlling the shape of the collector depletion layer which extends into the base region toward the emitter region.

Another feature of the invention is the provision of a transistor having a collector electrode separated from the emitter electrode by a base region of opposite conductivity type to the collector and emitter regions, with a layer embedded in the collector region having the same conductivity type as the base region which acts to shape the collector depletion layer so that it does not extend into the base region to engage the emitter with incrasing collector voltage.

A further feature of the invention is the provision of a transistor having a base region with an emitter region formed therein, and a collector region having a junction with the base region, wherein a lock layer is provided in the collector region for controlling the shape of the depletion layer formed in the base region, which has a portion extending to an external surface of the collector region for application of a control voltage thereto. By application of a control voltage to the lock layer, analog operation can be provided.

A still further feature of the invention is the provision of a transistor having a collector with a lock layer to control the shape of the collector depletion layer in the base region, so that the base region can be thinner, and which divides the capacity of the depletion layer so that the overall capacity is less, to thereby provide better high frequency operation.

The invention is illustrated in the drawing wherein:

FIG. 1 shows a transistor of usual construction and the collector depletion layer formed therein;

FIG. 2 illustrates a transistor in accordance with the invention having a lock layer in the collector region;

FIGS. 3A and 3B illustrate certain properties of the transistor of FIG. 2;

FIGS. 4A to 4E illustrate the steps of constructing the transistor of FIG. 2;

FIG. 5 illustrates a modified transistor construction in accordance with the invention; and

FIG. 6 illustrates certain properties of the transistor of FIG. 5.

In practicing the invention there is provided a transistor having base, emitter and collector regions, with the base region being of one conductivity type and the emitter and collector regions being of the opposite conductivity type. The transistor can be of either the NPN or the PNP type. The transistor includes a lock layer in the collector region which is spaced from the junction between the base and collector regions. The layer is of the same conductivity type as the base region, and acts to lock the position of the collector depletion layer formed when voltage is applied to the collector electrode with respect to the base electrode. When an increasing voltage is applied to the collector region, the collector depletion layer extends into the collector and base regions, until the depletion layer engages the lock layer. As the voltage is further increased, the depletion layer is shaped by the lock layer so that it does not extend farther into the base region, thus not engaging the emitter region to produce punch-through. The lock layer should be positioned with respect to the junction between the collector and base regions so that the depletion layer reaches the lock layer before it reaches the emitter region.

The lock layer in the collector electrode may be embedded within the electrode and have no external connection thereto. In an alternate construction, the lock layer may have a portion extending to an external surface of the collector electrode, so that a bias potential can be applied between the lock layer and the base region